ABSTRACT

The invention relates to a data processing system which comprises a memory module and a microprocessor. The memory modules comprise at least one low-speed memory and one high-speed memory; both store an interrupt vector table individually for recording the entry instruction of interrupt service routines. The microprocessor comprises a central processing unit (CPU) and a memory controller with a re-addressing device. Once an interruption occurs, the CPU generates and sends an interrupt vector address to the memory controller. If the vector is located in the range of interrupt vector table, the re-addressing device sends an enable signal to the high-speed memory to enable the CPU to fetch the entry instruction of interrupt service routines from the high-speed memory, not from the pre-determined low-speed memory. Hence, the interrupt latency is reduced.